

REMARKS

Claims 1-6 are currently pending in the instant application, with claim 6 added by this Amendment. Claims 1 and 4 are independent. Reconsideration of this application, as amended, is respectfully requested.

Objection to Drawings

The drawings were objected to by the Examiner for failing to include required descriptive wording. A Drawing Change Authorization Request along with proposed drawing changes to Figs. 1-5 and 7 shown in red are included herewith. Formal drawings will be submitted at a later date. Applicant submits that the objection to the drawings has been overcome and accordingly should be withdrawn.

Claim Rejections under 35 U.S.C. §112

Claims 1-5 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Office Action states that with respect to independent claim 1, a reception multiplexer has a reception processing means which transforms a plesiochronous signal into a synchronous signal. The

Office Action then states, however, that the signals received at the reception multiplexer have already been adapted to a common processing clock in a previous step and are thus synchronized or synchronous. Applicant submits that as disclosed in the application as originally filed, the clock synchronizer adapts the received plesiochronous signals to a common processing clock. Thereafter, the reception processing means further processes the time synchronized plesiochronous signals to provide signals at its output that are synchronous with respect to bit rate. Therefore, the circuit arrangement for a reception part of an SDH transmission system provides that signals output from the reception processing means are synchronous with respect to both a clock and a bit rate.

Further, the Office Action states that independent claim 4 recites that a transmission processing means transforms a synchronous signal into a plesiochronous signal. The Office Action then states, however, that the signal transmitted from the transmission processing means remains synchronized. Applicants submit that as disclosed in the application as originally filed, the transmission processing means *transforms* the transmitted synchronous signal into a plesiochronous signal. Thereafter, a desynchronizer following the transmission processing means *recovers* the plesiochronous signal clocks of the plesiochronous signals and issues the plesiochronous signals to a

plurality of output channels. Therefore, the circuit arrangement for a reception part of an SDH transmission system provides a transmission processing means for transforming the signals and a desynchronizer for recovering the signal clocks.

Thus, Applicant respectfully submits that claims 1 and 4 satisfy 35 U.S.C. §112, second paragraph, and this rejection should be withdrawn.

Claim Rejections under 35 U.S.C. §102

Claim 1 stands rejected under 35 U.S.C. §102(e) as being unpatentable over Chen et al. (U.S. Patent No. 5,940,456). The rejection is respectfully traversed.

Chen et al. teaches a plesiochronous digital hierarchy (PDH) system that allows for multiple bundles of PDH payload data streams to be synchronously transmitted from one point to another. The system includes a plurality of PDH multiplexers in a first stage that provide multiplexing to accommodate phase variations in tributary inputs. A synchronous clock is provided that synchronizes the PDH multiplexers. Thereafter, all tributaries at higher level multiplexing are synchronized using a synchronous multiplexer.

There is no teaching or suggestion within the Chen et al. patent document that approaches the limitations of independent claim 1. In

particular, Chen et al. fails to teach or suggest at least "reception processing means ... transforming a plesiochronous signal into a synchronous signal for an SDH transmission channel." Chen et al. teaches synchronizing PDH data streams using a synchronous PDH (plesiochronous digital hierarchy) system (i.e., synchronizing only the clock rate of the plesiochronous signals) to provide synchronized PDH data. However, Chen et al. fails to teach synchronizing SDH data streams, which requires synchronizing the clock rate and the bit rate. This provides advantages over the PDH system taught in Chen et al., and in particular, accommodates different kinds of systems and provides more functionality. Thus, Chen et al. only discloses a synchronous PDH system and does not disclose providing a synchronous signal for an SDH transmission channel. Therefore, Applicant respectfully submits that Chen et al. fails to disclose each and every element as required by claim 1 and the rejection under 35 U.S.C. §102(e) is improper.

Further, and with respect to newly added claim 6, in combination with the a circuit arrangement for a reception part of an SDH transmission system as claimed in claim 1, a synchronizer and mapper are not disclosed in the cited prior art. This provides a synchronous signal that is synchronized with respect to a bit rate as well to a clock, and which is not disclosed in the cited prior art. In particular, Chen et al. teaches away from this requirement. Chen et al. states that "there is

no need to do these stuffing and destuffing processing at every stage of the multiplexing" referring to the mapping needed in an SDH system. Thus, a synchronizer and mapper, and providing synchronization of both clock and bit rate are not taught in Chen et al. Thus, this claim is likewise allowable.

Claim Rejections under 35 U.S.C. §103(a)

Claims 1-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Graves (U.S. Patent No. 4,667,324). The rejection is respectfully traversed.

Graves discloses a time-division multiplexed digital transmission system that utilizes single stage multiplexing and demultiplexing for both synchronous and/or asynchronous bit streams from tributaries of widely differing bit rates. The invention provides for bit stuffing each of the tributaries to establish a harmonic relationship at the channel level and then at the tributary level of all the bitstreams being multiplexed. Graves discloses that various combinations of synchronous and/or asynchronous bit streams may be combined in a single stage multiplexer.

There is no teaching or suggestion within the Graves patent document that approaches the limitations of the claims. In particular, Graves fails to teach or suggest at least "reception processing means ...

for transforming a plesiochronous signal into synchronous signal for an SDH transmission channel" as set forth in claim 1, and "a transmission processing means for transforming a transmitted synchronous signal into a plesiochronous signal" as set forth in claim 4. As stated in the Office Action, Graves does note that the predetermined input rate and output rate can vary depending upon design preferences. However, Graves does not teach or suggest how to provide a reception processing means or transmission processing means as required by the claimed invention to provide signals that are synchronous with respect to clock and bit rate. It is not a matter of design choice to synchronize the bit rate to accommodate an SDH signal. The Office Action has not met the burden of showing where the Graves patent document make obvious the modification of the Graves to provide the claimed invention. Graves is concerned with transmissions using Pulse Code Modulated (PCM) signals and not SDH signals. There is no teaching in Graves that would make obvious the modification of the Graves system from one operating in connection with PCM signals to one operating in connection with SDH signals.

Therefore, Applicant respectfully submits that Graves et al. fails to disclose, either explicitly or implicitly each and every limitation of independent claims 1 and 4, and the rejection based upon 35 U.S.C §103(a) is improper. Further, claims 2 and 3, and newly added claim 6

depend from claim 1, and claim 5 depends from claim 4, and are likewise allowable for the same reasons that independent claims 1 and 4 are allowable.

CONCLUSION

Accordingly, in view of the above amendments and remarks, and all of the stated grounds of rejection having been properly traversed, accommodated, and/or rendered moot, reconsideration of the rejections of claims 1-5 and allowance of claims 1-5 and newly added claim 6 in connection with the present application is earnestly solicited. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is condition for allowance.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact the undersigned at (703) 390-3359 in order to discuss the present application.

Pursuant to 37 C.F.R. 1.17 and 1.136(a), the Applicant respectfully petitions for a one (1) month extension of time for filing a response in connection with the present application, and the required fee of \$110.00 is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. 1.16 or under 37 C.F.R. 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE,

P.L.C.

By: 

Gary D. Yacura

Registration No. 35,416

GDY/ERS:jcp

12355 Sunrise Valley Drive
Reston, Virginia 20191
703-390-3030



1/7

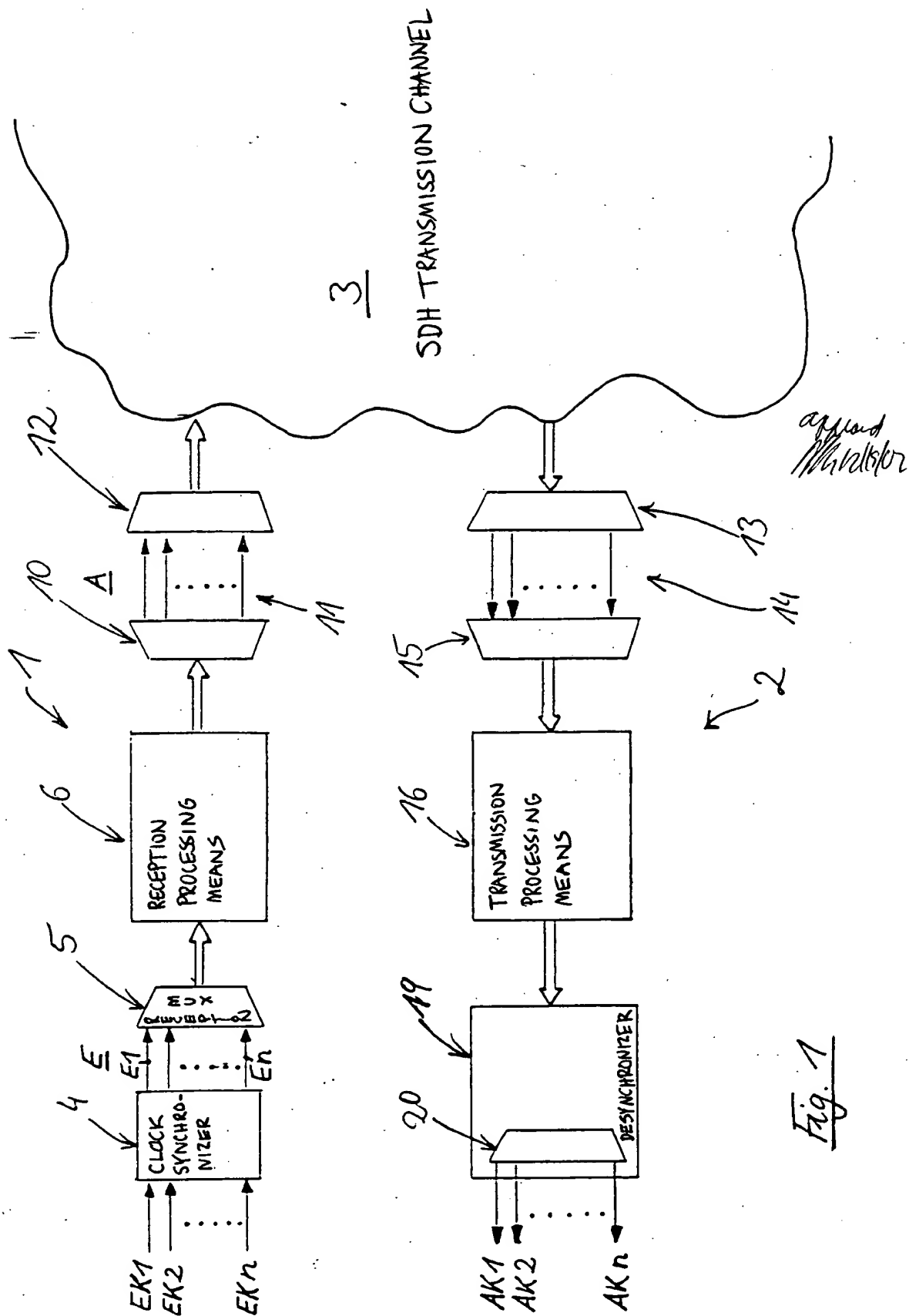


Fig. 1



2/7

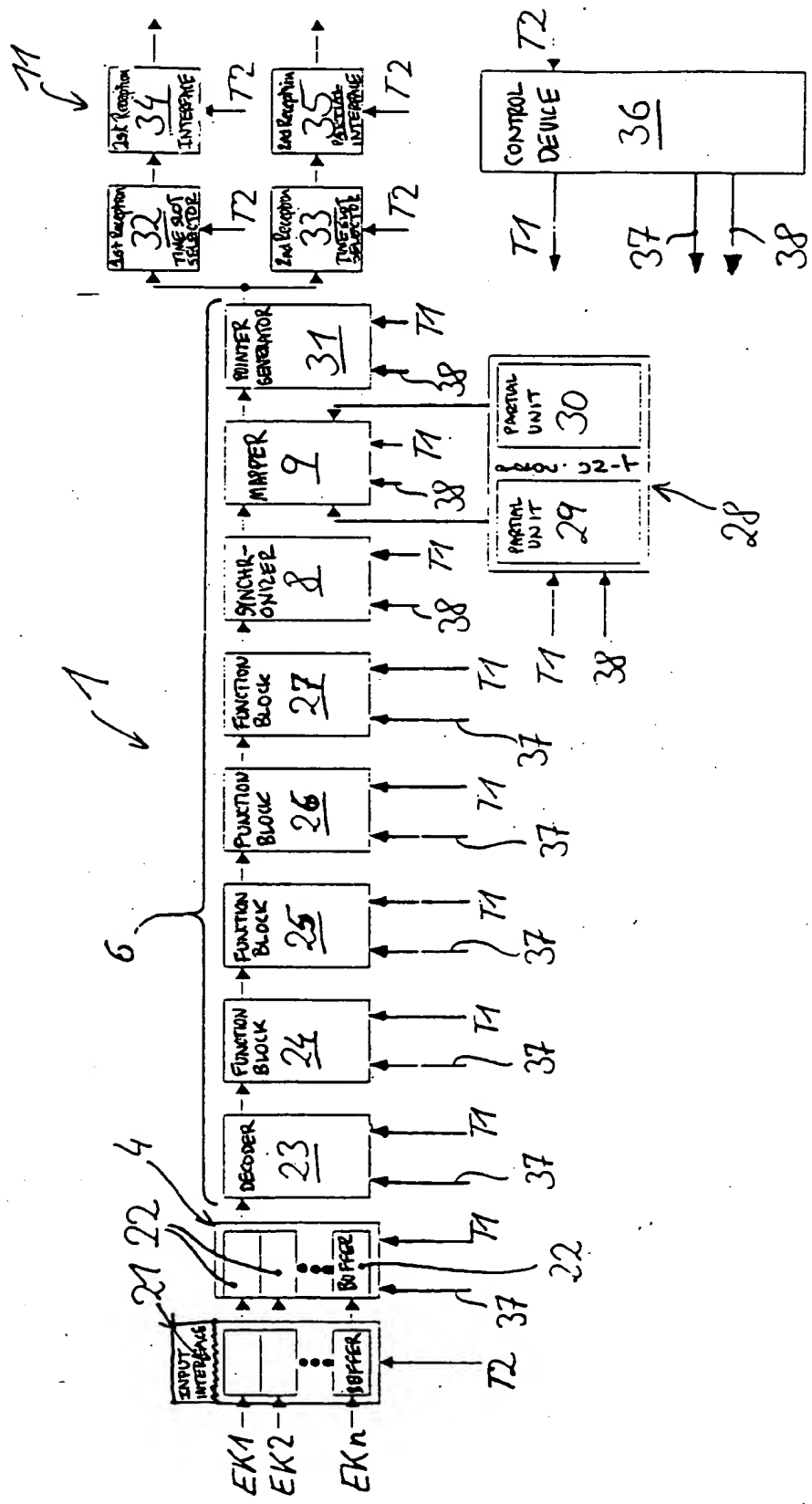


Fig. 2



3/7

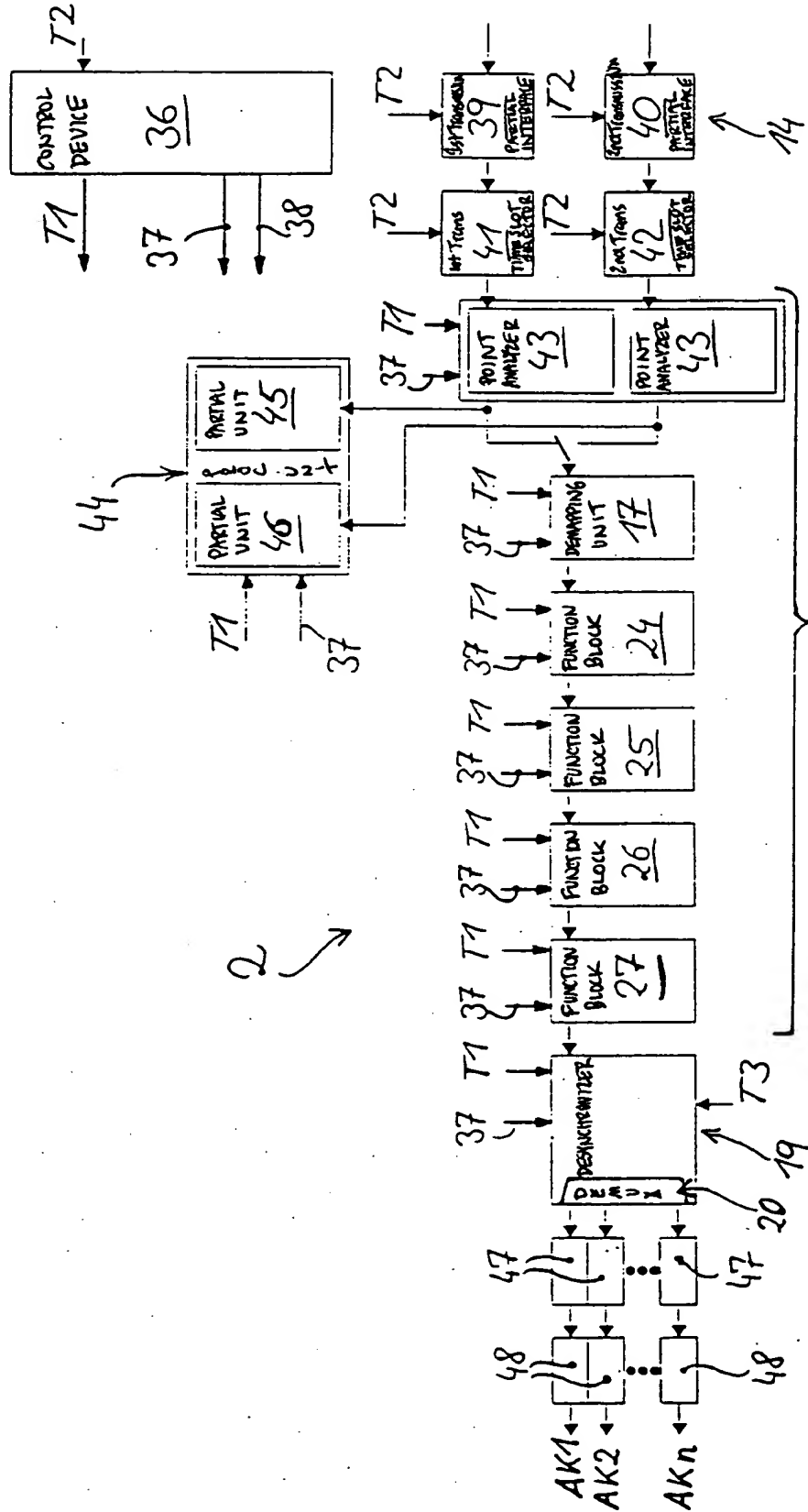


Fig. 3

Fig. 4

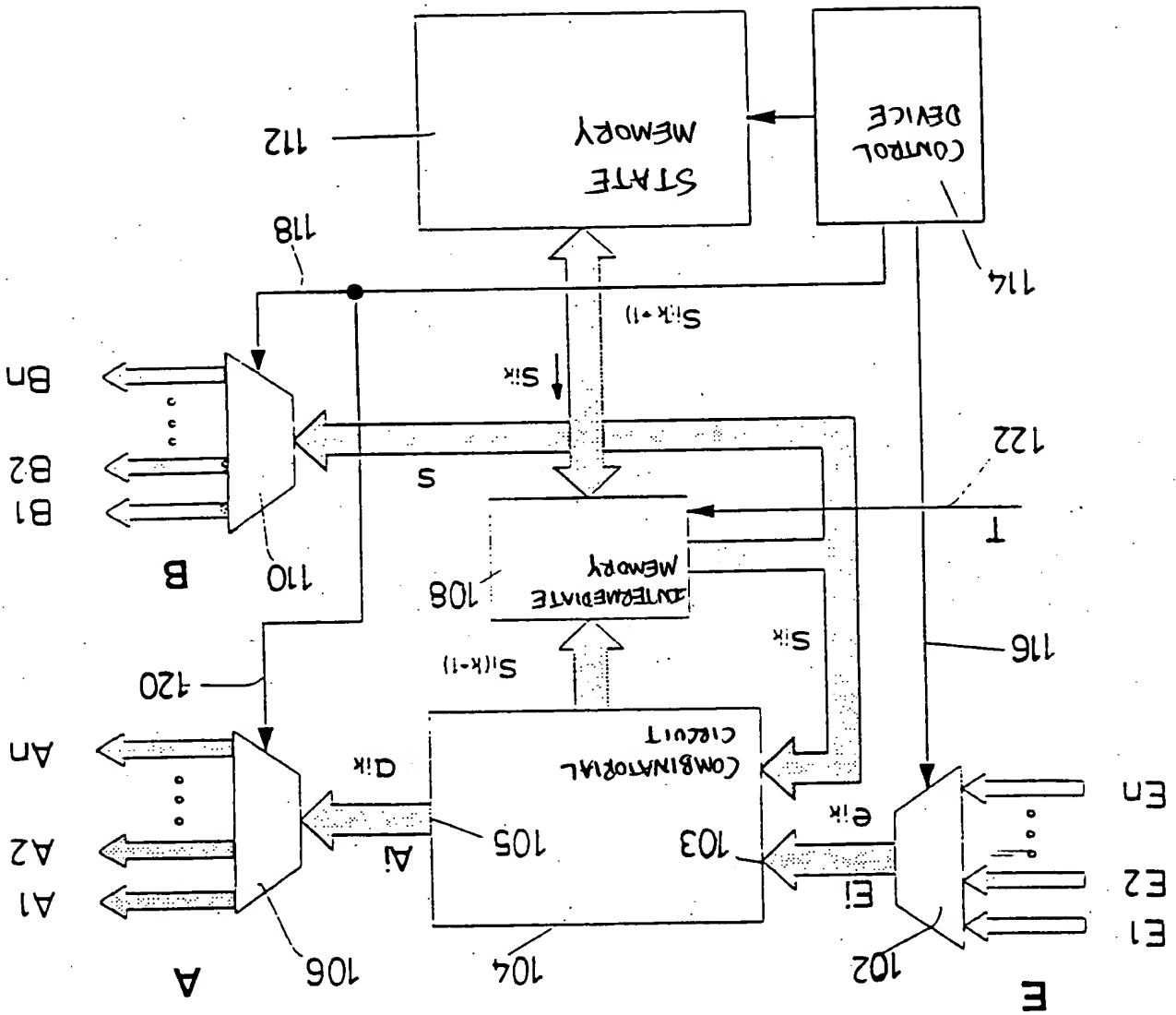




Fig. 5

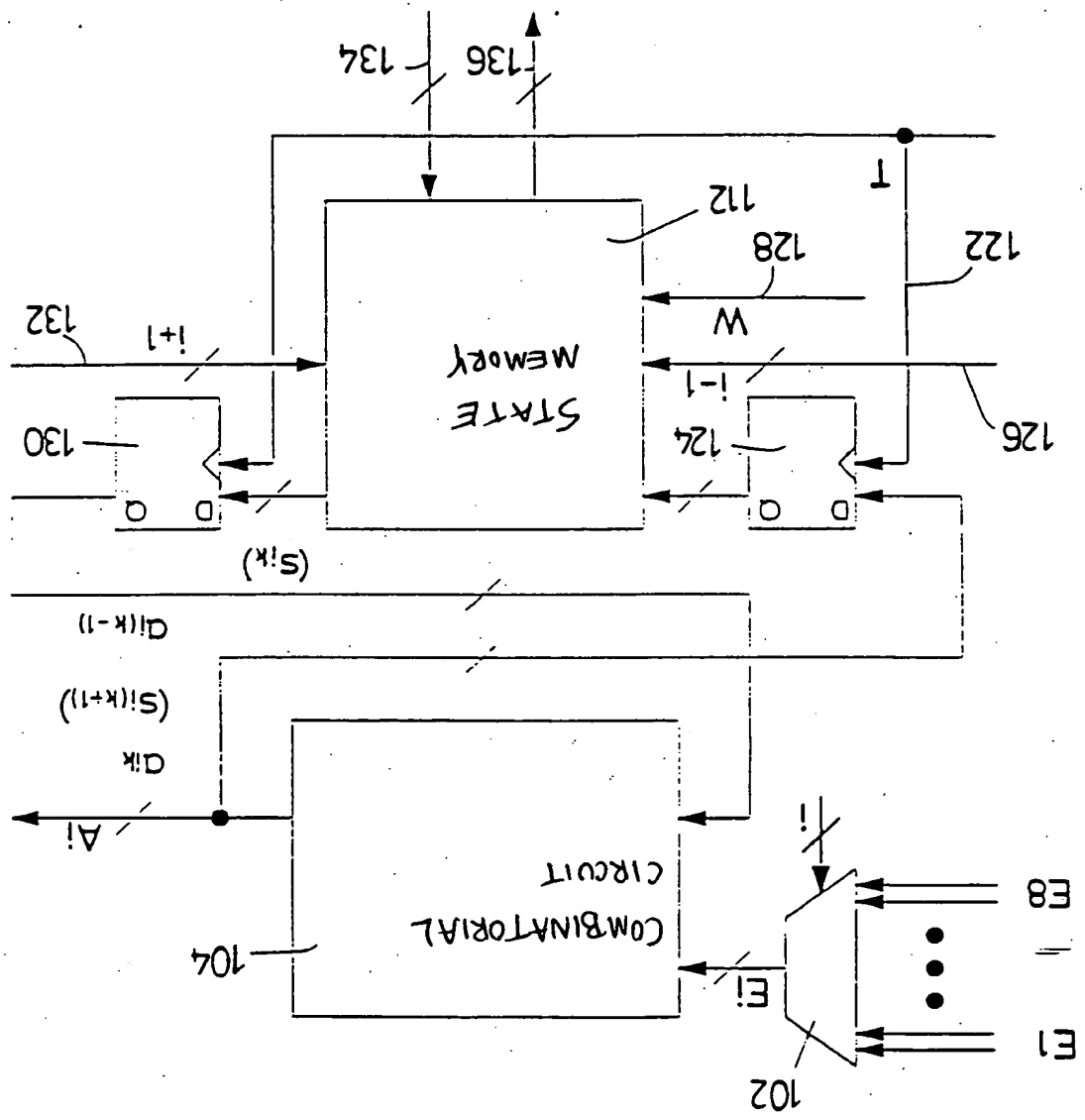




Fig. 7

